1. A method writing data into a static memory device comprising the steps of:

inputting data to be written into a memory cell, the memory cell being connected to first and second bit lines;

generating first and second currents in response to the input data; and

applying the first and second currents onto the bit lines, wherein said first and second currents represent a value of the input data or a tri-state condition.

2. The method of claim 1 further comprising the step of biasing the bit lines to a predetermined voltage level when a write operation is not being performed.

3. The method of claim 1 further comprising the step of biasing the bit lines to a predetermined voltage level when a read operation or a write operation is not being performed.

4. The method of claim 2 wherein the predetermined voltage is smaller than a first voltage used to power the memory device, but more than half of the first voltage.

5. The method of claim 5 wherein the predetermined voltage is approximately fifty-five percent of the first voltage.

6. The method of claim 1, wherein said generating step comprises:

switching in first and second adjustable resistive elements; and

applying respective first and second voltages to the first and second first and second adjustable resistive elements.

7. The method of claim 6 further comprising the step of adjusting the first and second adjustable resistive elements.

8. A method of reading data from a static memory device comprising the steps of:

sensing first and second currents from respective first and second bit lines connected to a memory cell of the device;

converting the sensed first and second currents into a voltage level representing a logical value of a content of the cell.

9. The method of claim 8 wherein said sensing step comprises:

biasing the bit lines to a predetermined voltage;

discharging one of the bit lines based on the content of the memory cell; and

sensing the current on the bit lines.

10. The method of claim 8 wherein said sensing step comprises:

biasing the bit lines to a predetermined voltage;

charging one of the bit lines based on the content of the memory cell; and

sensing the current on the bit lines.

11. The method of claim 8 further comprising the step of latching the logical value until the next read operation is performed on the cell.

12. A differential write driver for a static memory circuit, said write driver comprising:

an input circuit connected to a memory cell via first and second bit lines, said input circuit inputting data to be written into a memory cell; and

a current generating circuit connected to said input circuit, said current generating circuit generating first and second currents in response to the input data and applying the first and second currents onto the bit lines, said first and second currents representing a value of the input data or a tri-state condition.

13. The write diver of claim 12, further comprising a biasing circuit coupled to said bit lines, said biasing circuit biasing the bit lines to a predetermined voltage level when a write operation is not being performed.

14. The write driver of claim 13, wherein the predetermined voltage is smaller than a first voltage used to power the driver, but more than half of the first voltage.

15. The write driver of claim 14, wherein the predetermined voltage is approximately fifty-five percent of the first voltage.

16. The write driver of claim 12 further comprising a biasing circuit coupled to said bit lines, said biasing circuit biasing the bit lines to a predetermined voltage level when a read operation or a write operation is not being performed.

17. The write driver of claim 16, wherein the predetermined voltage is smaller than a first voltage used to power the driver, but more than half of the first voltage.

18. The write driver of claim 17, wherein the predetermined voltage is approximately fifty-five percent of the first voltage.

19. The write driver of claim 12, wherein said generating circuit comprises:

a first adjustable resistive element connected to a first voltage, a resistance of said first adjustable resistive element being controllable by a first control signal;

a second adjustable resistive element connected to a second voltage, a resistance of said second adjustable resistive element being controllable by a second control signal;

a first switch for switching in the resistance of the first adjustable resistive element in response to a third control signal; and

a second switch for switching in the resistance of the second adjustable resistive element in response to a fourth control signal,

wherein said first voltage is applied to said first adjustable resistive element and said second voltage is applied to said second adjustable resistive element when said third and fourth control signals are received.

20. The write driver of claim 19, wherein the fourth control signal is a complement of the third control signal.

21. The write driver of claim 20, wherein said third control signal is an enable signal and the fourth control signal is a complement of the enable signal.

22. The write driver of claim 19 further comprising a current loop generating circuit for generating the first and second control signals based on a reference voltage and a resistance of said current loop generating circuit.

23. The write driver of claim 12 wherein said input circuit further comprises an input logic circuit for inputting the data and first and second control signals, wherein said first and second control signals are used to determine if a read or write operation is in progress.

24. The write driver of claim 12, further comprising a biasing circuit comprising:

a first resistive element coupled between a first voltage and the first bit line;

a second resistive element coupled between a second voltage and the second bit line; and

a third resistive element coupled between the first and second bit lines, wherein said resistive elements are controlled to produce a predetermined voltage level on said bit lines when a write operation is not being performed.

25. The write driver of claim 24, wherein said biasing circuit further comprises a bit line reference and said bit line reference is used to generate said predetermined voltage.

26. A current sensing receiver circuit for a static memory device comprising:

a current sensing circuit connected to first and second bit lines, said current sensing circuit respectively sensing first and second currents from said first and second bit lines, said bit lines being connected to a memory cell of the device; and

a conversion circuit coupled to said first and second currents, said conversion circuit converting the first and second currents into a voltage level representing a logical value of a content of the cell.

27. The current sensing receiver of claim 26 wherein said conversion circuit comprises a flip-flop circuit.

28. The current sensing receiver of claim 27 wherein the flip-flop circuit latches the logical value until the next read operation is performed on the cell.

29. The current sensing receiver of claim 26 wherein said conversion circuit comprises:

a first latching circuit coupled to said first and second currents; and

a second latching circuit coupled to the output of said first latching circuit, wherein said first latch circuit converts the first and second currents into the voltage level representing the logical value of the content of the cell and said second latching circuit maintains the logic value until the next read operation is performed on the cell.

30. A memory circuit comprising:

a memory cell;

an input circuit connected to said memory cell via first and second bit lines, said input circuit inputting data to be written into said memory cell;

a current generating circuit connected to said input circuit, said current generating circuit generating first and second currents in response to the input data and applying the first and second currents onto the bit lines during a write operation, said first and second currents representing a value of the input data or a tri-state condition;

a current sensing circuit connected to the first and second bit lines, said current sensing circuit respectively sensing third and fourth currents from the first and second bit lines during a read operation; and

a conversion circuit coupled to said third and fourth currents, said conversion circuit converting the third and fourth currents into a voltage level representing a logical value of a content of the cell.

31. A processor system comprising:

a processor;

a memory circuit connected to said processor, said memory circuit comprising a differential write driver for a static memory circuit, said write driver comprising:

an input circuit connected to a memory cell via first and second bit lines, said input circuit having first and second inputs for inputting data to be written into said memory cell; and

a current generating circuit connected to said first and second inputs, said current generating circuit generating first and second currents in response to the input data and applying the first and second currents onto the bit lines, said first and second currents representing a value of the input data or a tri-state condition.

32. The system of claim 31, wherein said write driver further comprises a biasing circuit coupled to said bit lines, said biasing circuit biasing the bit lines to a predetermined voltage level when a write operation is not being performed.

33. The system of claim 32, wherein the predetermined voltage is smaller than a first voltage used to power the driver, but more than half of the first voltage.

34. The system of claim 32, wherein the predetermined voltage is approximately fifty-five percent of the first voltage.

35. The system of claim 31, wherein said write driver further comprises a biasing circuit coupled to said bit lines, said biasing circuit biasing the bit lines to a predetermined voltage level when a read operation or a write operation is not being performed.

36. The system of claim 35, wherein the predetermined voltage is smaller than a first voltage used to power the driver, but more than half of the first voltage.

37. The system of claim 35, wherein the predetermined voltage is approximately fifty-five percent of the first voltage.

38. The system of claim 31, wherein said generating circuit comprises:

a first adjustable resistive element connected to a first voltage, a resistance of said first adjustable resistive element being controllable by a first control signal;

a second adjustable resistive element connected to a second voltage, a resistance of said second adjustable resistive element being controllable by a second control signal;

a first switch for switching in the resistance of the first adjustable resistive element in response to a third control signal; and

a second switch for switching in the resistance of the second adjustable resistive element in response to a fourth control signal,

wherein said first voltage is applied to said first adjustable resistive element and said second voltage is applied to said second adjustable resistive element when said third and fourth control signals are received.

39. The system of claim 38, wherein the fourth control signal is a complement of the third control signal.

40. The system of claim 38, wherein said third control signal is an enable signal and the fourth control signal is a complement of the enable signal.

41. The system of claim 38, wherein said write driver further comprises a current loop generating circuit for generating the first and second control signals based on a reference voltage and a resistance of said current loop generating circuit.

42. The system of claim 31 wherein said input circuit further comprises an input logic circuit for inputting the data and first and second control signals, wherein said first and second control signals are used to determine if a read or write operation is in progress.

43. The system of claim 31, wherein said write driver further comprises a biasing circuit comprising:

a first resistive element coupled between a first voltage and the first bit line;

a second resistive element coupled between a second voltage and the second bit line; and

a third resistive element coupled between the first and second bit lines, wherein said resistive elements are controlled to produce a predetermined voltage level on said bit lines when a write operation is not being performed.

44. The system of claim 43, wherein said biasing circuit further comprises a bit line reference and said bit line reference is used to generate said predetermined voltage.

45. A processor system, comprising:

a processor; and

a memory circuit connected to said processor, said memory circuit comprising a current sensing receiver circuit for a static memory device comprising:

a current sensing circuit connected to first and second bit lines, said current sensing circuit respectively sensing first and second currents from said first and second bit lines, said bit lines being connected to a memory cell of the device; and

a conversion circuit coupled to said first and second currents, said conversion circuit converting the first and second currents into a voltage level representing a logical value of a content of the cell.

46. The system of claim 45 wherein said conversion circuit comprises a flip-flop circuit.

47. The system of claim 46 wherein the flip-flop circuit latches the logical value until the next read operation is performed on the cell.

48. The system of claim 45 wherein said conversion circuit comprises:

a first latching circuit coupled to said first and second currents; and

a second latching circuit coupled to the output of said first latching circuit, wherein said first latch circuit converts the first and second currents into the voltage level representing the logical value of the content of the cell and said second latching circuit maintains the logic value until the next read operation is performed on the cell.

49. A memory circuit comprising:

a static memory cell connected to first and second bit lines;

an input circuit, said input circuit having first and second inputs, said inputs corresponding inputting data to be written into a memory cell; and

a current generating circuit connected to said input circuit, said current generating circuit generating first and second currents in response to the input data and applying the first and second currents onto the bit lines, said first and second currents representing a value of the input data or a tri-state condition.

50. The memory circuit of claim 49, further comprising a biasing circuit coupled to said bit lines, said biasing circuit biasing the bit lines to a predetermined voltage level when a write operation is not being performed.

51. The memory circuit of claim 49, further comprising a biasing circuit coupled to said bit lines, said biasing circuit biasing the bit lines to a predetermined voltage level when a read operation or a write operation is not being performed.

52. The memory circuit of claim 51, wherein the predetermined voltage is smaller than a first voltage used to power the driver, but more than half of the first voltage.

53. The memory circuit of claim 49, wherein said generating circuit comprises:

a first adjustable resistive element connected to a first voltage, a resistance of said first adjustable resistive element being controllable by a first control signal;

a second adjustable resistive element connected to a second voltage, a resistance of said second adjustable resistive element being controllable by a second control signal;

a first switch for switching in the resistance of the first adjustable resistive element in response to a third control signal; and

a second switch for switching in the resistance of the second adjustable resistive element in response to a fourth control signal,

wherein said first voltage is applied to said first adjustable resistive element and said second voltage is applied to said second adjustable resistive element when said third and fourth control signals are received.

54. The memory circuit of claim 53, further comprising a current loop generating circuit for generating the first and second control signals based on a reference voltage and a resistance of said current loop generating circuit.

55. The memory circuit of claim 49, wherein said input circuit further comprises an input logic circuit for inputting the data and first and second control signals, wherein said first and second control signals are used to determine if a read or write operation is in progress.

56. The memory circuit of claim 49, further comprising a biasing circuit comprising:

a first resistive element coupled between a first voltage and the first bit line;

a second resistive element coupled between a second voltage and the second bit line; and

a third resistive element coupled between the first and second bit lines, wherein said resistive elements are controlled to produce a predetermined voltage level on said bit lines when a write operation is not being performed.

57. The memory circuit of claim 49, wherein the memory cell is a static random access memory cell.

58. The memory circuit of claim 49, wherein the memory cell is a content addressable memory cell.

59. A memory circuit comprising:

a static memory cell connected to first and second bit lines;

a current sensing circuit connected to said first and second bit lines, said current sensing circuit respectively sensing first and second currents from said first and second bit lines; and

a conversion circuit coupled to said first and second currents, said conversion circuit converting the first and second currents into a voltage level representing a logical value of a content of said cell.

60. The memory circuit of claim 59, wherein said conversion circuit comprises a flip-flop circuit that latches the logical value until the next read operation is performed on the cell.

61. The memory circuit of claim 59, wherein said conversion circuit comprises:

a first latching circuit coupled to said first and second currents; and

a second latching circuit coupled to the output of said first latching circuit, wherein said first latch circuit converts the first and second currents into the voltage level representing the logical value of the content of the cell and said second latching circuit maintains the logic value until the next read operation is performed on the cell.

62. A network router comprising:

a processor; and

a content addressable memory device connected to said processor, said content addressable memory comprising:

a content addressable memory cell;

an input circuit connected to input data to be written into said memory cell;

a current generating circuit connected to said input circuit, said current generating circuit generating first and second currents in response to the input data and applying the first and second currents onto the bit lines during a write operation, said first and second currents representing a value of the input data or a tri-state condition;

a current sensing circuit connected to the first and second bit lines, said current sensing circuit respectively sensing third and fourth currents from the first and second bit lines during a read operation; and

a conversion circuit coupled to said third and fourth currents, said conversion circuit converting the third and fourth currents into a voltage level representing a logical value of a content of the cell.